CLAIMS

1. A memory redundancy circuit in a memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure, the memory redundancy circuit, comprising:

a. a redundant group of memory cells; and

b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.

2. The memory redundancy circuit of Claim 2, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

3. The memory redundancy circuit of Claim 2, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

4. The memory redundancy circuit of Claim 3, wherein the plurality of selectable switches are fuses.

5. The memory redundancy circuit of Claim 4, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

6. The memory redundancy circuit of Claim 1, wherein each of the designated group of memory cells and the redundant group of memory cells comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

7. A memory circuit comprising:

at least one designated memory cell;

at least one redundant memory cell; and

a controller that redirects a signal path from the at least one designated memory cell to the at least one redundant memory cell based on a failure of the at least one designated memory cell.

8. The memory circuit of claim 7 wherein the controller comprises a decoder responsive to an encoded signal representative of failure of the at least one designated memory cell.

9. The memory circuit of claim 8, wherein the controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the encoded signal.

10. The memory redundancy circuit of Claim 3, wherein the plurality of selectable switches are fuses.

11. The memory circuit of Claim 7, wherein the at least one designated memory cell and the at least one redundant memory cell each comprise one of a row of memory

cells, a column of memory cells, a row pair of memory cells, and a column pair of memory cells.

12. The memory circuit of Claim 10, wherein the at least one designated memory cell and the at least one redundant memory cell each comprise a line pair of memory cells, and wherein a number of fuses is logarithmically related to a number of line pairs.

13. A memory circuit comprising:

at least one line of designated memory cells;

at least one line of redundant memory cells; and

a controller that redirects a signal path from the at least one line of designated memory cells to the at least one line of redundant memory cells based on a failure of the at least one line of designated memory cells.

14. The memory circuit of claim 13 wherein the controller comprises a decoder responsive to an encoded signal representative of the failure of the at least one line of designated memory cells.

15. The memory circuit of Claim 14, wherein the controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the encoded signal.

16. The memory redundancy circuit of Claim 15, wherein the plurality of selectable switches are fuses.

17. The memory circuit of Claim 13, wherein the at least one line of designated memory cells and the at least

one line of redundant memory cells each comprise one of a row of memory cells, a column of memory cells, a row pair of memory cells, and a column pair of memory cells.

18. The memory circuit of Claim 10, wherein the at least one line of designated memory cells and the at least one line of redundant memory cells each comprise a line pair of memory cells, and wherein a number of fuses is logarithmically related to a number of line pairs.

19. A memory circuit comprising:

a plurality of designated memory cells;

a plurality of redundant memory cells; and

at least one fuse box that utilizes a single output to cause a signal path from the plurality of designated memory cells to be redirected to the plurality of redundant memory cells based on a failure of the plurality of designated memory cells.

20. The memory circuit of claim 19 wherein the fuse box generates an encoded signal representative of the failure of the at least one line of designated memory cells.

21. The memory circuit of Claim 19, wherein the plurality of designated memory cells and the plurality of redundant memory cells each comprise one of a row of memory cells, a column of memory cells, a row pair of memory cells, and a column pair of memory cells.

22. The memory circuit of Claim 19, wherein the plurality of designated memory cells and the plurality of redundant memory cells each comprise a line pair of memory

cells, and wherein a number of fuses in the at least one fuse box is logarithmically related to a number of line pairs of memory cells.

5